AN2132
Application note

STLC3075 very low single supply SLIC for WLL application in flyback configuration

Introduction

The STLC3075 is a SLIC device specially designed for WLL (Wireless Local Loop) and ISDN terminal adapters.

This document contains a description of the device functions in flyback configuration, and provides some application hints. The device data sheet is an essential complement to this application note, providing important reference information that will simplify understanding of the content.

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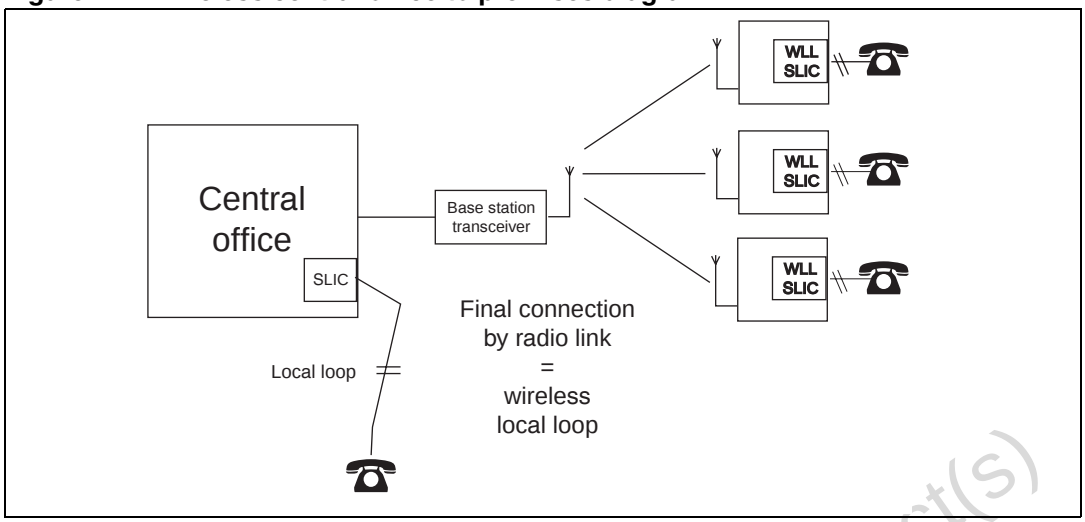
1 Wireless local loop system

Figure 1. Wireless central office to premises diagram



The main characteristics of this device consist in the possibility to:

- operate with a single supply voltage in **Fly-Back** or **Buck-Boost** configuration (see AN2118 for information on Buck-Boost configuration)
- operate in **Fly-Back** configuration with a single supply voltage VPOS in a range from +4.5 V to +12 V
- generate negative battery voltage
- generate a ring signal (trapezoidal wave form)

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2 Packaging

STLC3075 is housed in standard TQFP package plastic with copper lead frame. No copper slugs protrude from the plastic body. STLC3075 uses the “standard” package option.

The thermal resistances, shown in *Table 1* and *Figure 2*, are considered between the junction and the ambient still air, and are calculated or measured in ° C/W.

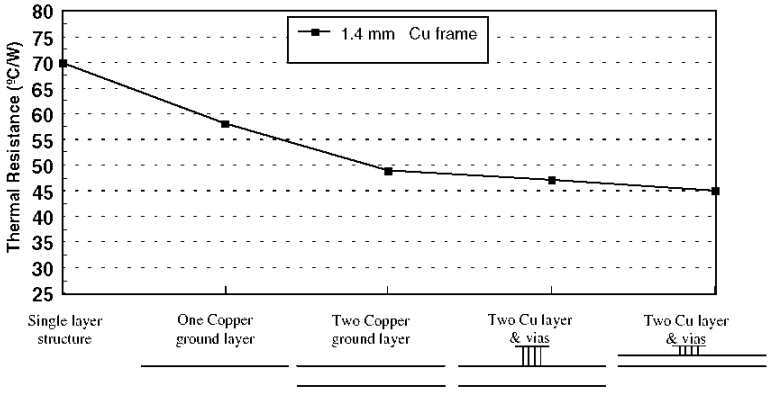
Table 1. Thermal resistance versus package size

Symbol	Parameter	Value	Unit
Rth j-amb	Thermal resistance junction ambient (Full plastic TQFP on single layer board)	70	° C/W
Rth j-amb	Thermal resistance junction ambient (Full plastic TQFP on four layer board)	45	° C/W

2.1 TQFP 10 mm x 10 mm x 1.4 mm

Theta (j-a) on boards, in still air

Figure 2. Thermal resistance versus board structure



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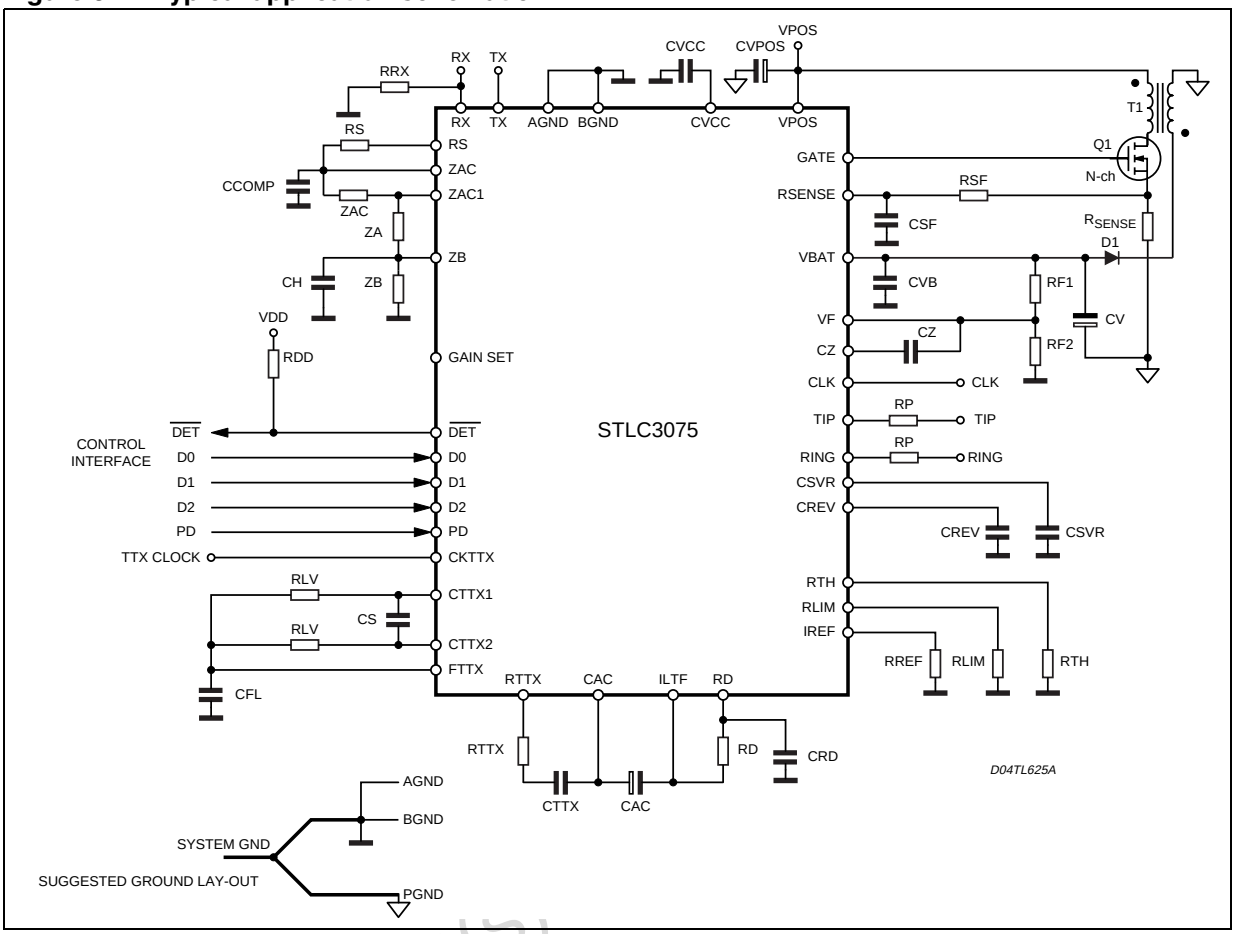
3 Application information

Figure 3. Typical application schematic



3.1 VBAT voltage generation

When operated with a positive supply voltage VPOS and a correctly set clock signal (typically 125 kHz), the SLIC generates a VBAT voltage for the active and ring operations.

The VBAT voltage level, with a 10% spread, is defined by the voltage divider RF1 / RF2 and can be set by choosing an RF1 value from a recommended set of values (see *Table 2*):

Table 2. VBAT voltage values (VPOS = 4.5V)

RF1 (KΩ)	VBAT (Active mode)	VBAT (Ring mode)
270	-46.1V	-64.4V
285	-48.4V	-67,8V
300	-51.9V	-71.7V
315	-54.3V	-75.2V
330	-56.3V	-78.2V

Obsolete Product(s)

These values are referred to the device in active mode, on-hook condition (IL = 0mA) and in ring mode without load.

The VBAT value must be chosen taking into account the absolute maximum ratings of the device (VBTOT = 90 V). VBTOT = (VBAT + VPOS) = 90 V must not be exceeded.

When ring mode is selected through the control interface, the VBAT voltage is increased by an internal circuit from it's active level to a predetermined value for ring mode. These two voltage levels (VBAT active and VBAT ring) are hence correlated. When one is set, (ring or active), the other is also set at the same time.

3.2 Operation in off-hook condition

A major feature of this device is that when changing from on-hook to off-hook conditions (IL >0 mA), the VBAT voltage is automatically adjusted depending on the loop resistance and on the programmed current limitation value (ILIM).

It should be noted that the device is optimized to operate on short loop applications (RLOOP ≤500 Ω) in order to obtain the correct ring-trip detection.

In these conditions, with line current reaching the programmed constant current feed value (ILIM), the STLC3075 works like a current generator with a fixed DC current.

A fixed voltage drop, 4 V on TIP/GND and approximately 6 V on RING/VBAT, assures the DC functionality and the proper swing for the AC signal.

When the line is set off-hook, the STLC3075 automatically adjusts the generated battery voltage (VBAT) to feed the line with a fixed DC current (programmable via RLIM), and so optimizes power dissipation.

Considering maximum and minimum values for RLOOP ranging from 500 to100 Ω, and with fixed parameters ILIM = 25 mA and 2Rp = 100 Ω, the battery voltage (VBAT) will be equal to:

1. VBAT = 25 mA x (500+100) + 10 V = - 25 V
2. VBAT = 25 mA x (100+100) + 10 V = - 15 V

A correctly set current threshold (typically 9 mA), programmable by external resistor RTH, allows the correct on/off hook transition function.

During the off-hook dynamic transition, the CAC capacitor is charged. The line current regulator system senses the current flowing into RD and reduces the ILOOP current to the programmed ILIM value, set by RLIM.

The settling time of the ILIM current is about 150 ms, and it is a function of the CAC splitter capacitor (min. value allowed is 22 µF).

3.3 VPOS characteristics

The input voltage VPOS can change slowly within the data sheet range (4.5 V - 12 V) without any effect on the VBAT voltage.

The STLC3075 can continue to operate correctly even if the VPOS voltage occasionally goes below 4.5 V (instantaneous value, not steady-state). The only limitation is the minimum voltage required on the external PMOS to keep it in a linear area.

Fast transients, ripples and spikes on the supply voltage V_{POS} will appear on TIP/RING with a reduced amplitude, depending upon the voltage supply rejection of the device.

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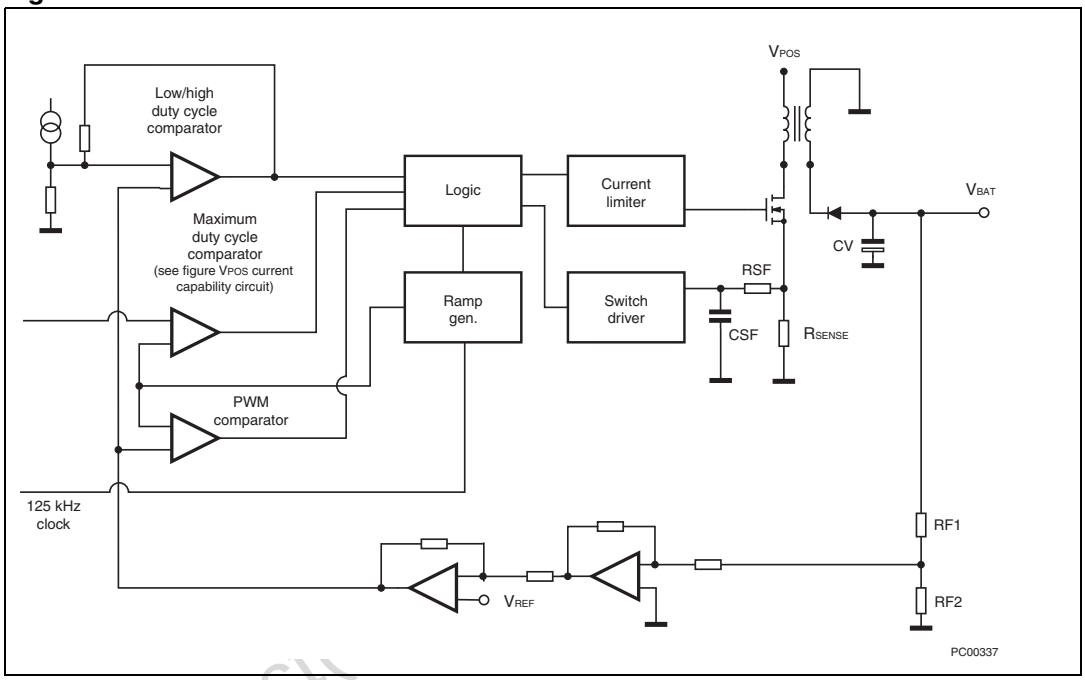
Bench measurements on SVRR give -35 dB @ f = 50 Hz and -47 dB @ f = 4 kHz, using the test circuit configuration with the device in active mode, loaded with an RLOOP = 500 Ω, and ILIM = 25 mA.

3.4 Start-up and DC-DC converter

In order to prevent problems during start-up, an internal circuit turns-on the gate of the MOSFET only when VPOS reaches 4 V and turns it off for VPOS lower than 3 V.

For VPOS voltage higher than 4 V the DC/DC converter power-on is controlled by a soft start circuit embedded on the devices.

Figure 4. DC-DC converter circuit



The DC/DC converter works in flyback condition using a two step process.

- During the ON-time of the MOSFET, energy is taken from the input and stored in the primary winding of the flyback transformer. On the secondary side, the diode is reverse biased, thus the load is being supplied by the energy stored in the output bulk capacitor.
- As soon as the power-mos turns off, the primary circuit is open and the energy stored in the primary is transferred to the secondary by magnetic coupling. The diode is forward biased, and the stored energy is delivered to the output capacitor and then on the load.

The dots on the transformer must be in accordance with the voltage, so that during the ON-time of the MOSFET they indicate the positive side with respect to the other one of the transformer. During MOSFET OFF-time they indicate the negative.

The MOSFET must be chosen with the correct Vds voltage rating, considering also the voltage reflected back (Vr) to the primary through the turns ratio **n**.

The reflected voltage (Vr) must be added to the input voltage VPOS giving out a much higher voltage on the drain of the Mosfet (VBAT / **n**) + VPOS.

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A MOSFET with a VDS greater than two times the VPOS voltage is recommended. The STN4NF03L, with a VDS of 30 V satisfies this parameter.

In the same way, the diode SMBYT01-400 with a VRRM of 400 V is able to operate properly considering a reverse voltage value calculated by VPOS x turns ratio + VBAT. In order to guarantee correct discharge timing to the transformer, avoiding possible saturation phenomenon, the max duty-cycle is limited to 60%, with a minimum duty-cycle of about 5%.

3.5 Suggested transformers

COEV magnetics type MGPWG-00007

Flyback transformer: 4 W; 1:16

To be used in VPOS range = 4.5 V/8.5 V

Table 3. Transformer Electrical specifications - VPOS range = 4.5V/ 8.5V(1)

Test description	Limit	Units	Tol.	Notes
Inductance	0.019	mH	+/- 8%	1-3, 10 kHz, 100 mVAC, Ls.
Leakage inductance	0.400	µH	Max.	1-3, 10 kHz, 10 mA, Ls.
DC resistance	0.101	Ω	Max.	1-3
DC resistance	19.50	Ω	Max.	4-6
Turns ratio	16:1	-	+/-4%	(4-6): (1-3), 10 kHz, 100 mVAC
Dielectric	1.500	VAC	500 µA	1-4, 1 second test, 500 µA max leakage current

1. @ +20° C unless noted otherwise

COEV magnetics type MGPWG-00008

Flyback transformer: 4 W; 1: 8

To be used in VPOS range = 8.5 V/12 V

Table 4. Electrical specifications - VPOS range = 8.5V/12V (1)

Test description	Limit	Units	Tol	Notes
Inductance	0.019	mH	+/- 8%	1-3, 10 kHz, 100 mVAC, Ls.
Leakage inductance	0.400	µH	Max.	1-3, 10 kHz, 10 mA, Ls.
DC resistance	0.101	Ω	Max.	1-3
DC resistance	5.83	Ω	Max.	4-6
Turns ratio	8: 1	-	+/-4%	(4-6): (1-3), 10 kHz, 100 mVAC
Dielectric	1.500	VAC	500 µA	1-4, 1 second test, 500 µA max leakage current

1. @ +20° C unless noted otherwise.

Obsolete Product(s) - Obsolete Product(s)

Table 5. Coilcraft type FA2469-AL electrical specifications

Test description	Limit	Unit	Tol	Notes
Inductance	0.0205	mH	Max	1-3, 10 kHz, 100 mVmrs
Leakage inductance	0.414	µH	Max	1-3, 100 kHz, 100 mVmrs short pins 4,6
DC resistance	0.036	Ω	Max	1-3
DC resistance	16.50	Ω	Max	4-6
Turns ratio	16:1	-	+/-4%	(4-6):(1-3), 10 kHz, 100 mVAC
HI POT	1.500	VAC		VDC to be applied for 1 second from pins 1,3 to pins 4,6. 500 µA max leakage current

Table 6. Coilcraft type FA2470-AL electrical specifications

Test description	Limit	Unit	Tol	Notes
Inductance	0.0205	mH	Max	1-3, 10 kHz, 100 mVmrs
Leakage inductance	0.40	µH	Max	1-3, 100 kHz, 100 mVmrs Short pins 4,6
DC resistance	0.036	Ω	Max	1-3
DC resistance	7.92	Ω	Max	4-6
Turns ratio	8:1	-	+/-3.3%	(4-6):(1-3), 10 kHz, 100 mVAC
HI POT	1.500	VAC		VDC to be applied for 1 second from pins 1,3 to pins 4,6. 500 µA max leakage current

Obsolete Product(s) - Obsolete Product(s)

3.6 Input current limitation

In WLL applications, the power supply usually does not have high-power current capability. Therefore when a ring trip occurs, the status of the SLIC changes from ring mode to off-hook condition. As the loop current control does not react immediately, the line current reaches the output stages current limitation value of about 80 mA.

As a consequence, a high peak current is sunk from VPOS which could be higher than its maximum current capability. In this case, if no limiting current circuit is used, (RSENSE = 0), the VPOS voltage would drop.

To prevent this, the STLC3075 incorporates a circuit to limit peak current on the VPOS input. The peak current value is defined by the formula:

$$IPEAK = \frac{375mV}{RSENSE}$$

This input current limitation circuit operates during all transients caused by changes in the line current conditions.

3.7 VPOS current capability

The following tables summarize the approximate value of the Ivpos current, drawn from the VPOS supply vs. REN 20Hz condition (For REN definition see section *3.10* below).

RSENSE = 0.22 mΩ

3.7.1 With USA REN

1REN (USA) = 8 µF + 6930 Ω

Transformer MGPWG-00007 for the VPOS range 4.5 V- 8 V.

Transformer MGPWG-00008 for the VPOS range 9.0 V-12 V

Table 7. Ivpos, average current (USA REN)

VPOS (V)	1REN	2REN	3REN	5REN
	Ivpos (mA)	Ivpos (mA)	Ivpos (mA)	Ivpos (mA)
4.5	185	340	520	750
6	145	260	360	640
8	115	145	270	440
9	100	180	240	400
10	90	150	220	330
12	80	130	180	280

Table 8. Ivpos, peak current (USA REN)

VPOS (V)	1REN	2REN	3REN	5REN
	Ivpos (mApk)	Ivpos (mApk)	Ivpos (mApk)	Ivpos (mApk)
4.5	800	1100	1300	1700
6	700	1000	1400	1800
8	800	1000	1400	1900
9	800	1100	1300	1900
10	800	1100	1300	1700
12	800	1100	1300	1700

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3.7.2 With European REN

1REN (Europe) = 1 µF+1800 Ω

Transformer MGPWG-00007 for the VPOS range 4.5 V- 8 V

Transformer MGPWG-00008 for the VPOS range 9.0 V-12 V

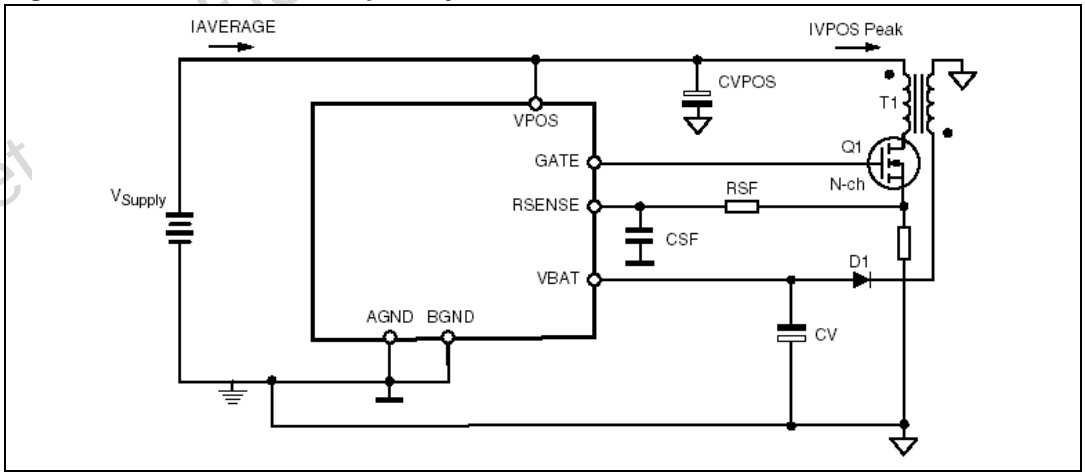
Table 9. Ivpos, average current (European REN)

VPOS (V)	1REN	2REN	3REN
	Ivpos (mA)	Ivpos (mA)	Ivpos (mA)
4.5	150	270	370
6	115	185	270
8	90	145	200
9	80	125	180
10	75	120	170
12	65	100	140

Table 10. Ivpos, peak current (European REN)

VPOS (V)	1REN	2REN	3REN
	Ivpos (mApk)	Ivpos (mApk)	Ivpos (mApk)
4.5	700	1900	1900
6	900	1300	1600
8	900	1300	1600
9	900	1300	1500
10	1000	1300	1500
12	1000	1300	1500

Figure 5. VPOS current capability circuit



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3.8 RSENSE setting

The RSENSE resistor sets the input peak current value, which must be lower than the power supply current capability limit.

In a typical application, the input peak current is fixed at 1.7 ApK (375 mV / 220 mΩ) in order to guarantee optimum performance in the total range of the current loop (20 to 40 mA) and the V_{POS} supply (4.5 to 12 V), driving up to 5REN of load.

3.9 Trapezoidal ringing signal

In the application domain targeted for this product (Integrated Access Device, Set Top Box, Small Office Home Office etc....) non sinusoidal ring waveforms are accepted. Therefore the STLC3075 generates ringing signals with a trapezoidal waveform.

This type of waveform is very similar to a sine wave whose distortion can be kept lower than 5% and crest factors have a value of 1.2, just by correct selection of the external CREV capacitor.

Because the value of CREV is a function of the ringing frequency, this value has to be adapted to the ringing frequency used.

A CREV in the range 18 to 22 nF gives a trapezoidal ringing signal and correct shaping with 20 to 25 Hz ringing frequency. To increase the ringing frequency to 68 Hz, the value of CREV should be chosen in the range of 6.8 to 8.2 nF.

3.10 Ringer load

3.10.1 With European REN

In a typical application the STLC3075 can drive up to 3REN european standard (1REN = 1800 Ω + 1 µF), @ f = 20 Hz, with crest factor (VppK / Vrms) = 1.22. The levels measured at the ringer terminal are summarized in the following tables.

Table 11. Ringer load (VPOS = 4.5 V) with European REN

CREV	Crest factor	1 REN		3 REN	
		Vppk	Vrms	Vppk	Vrms
22nF	1.22	65.6V	53.5V	64.8V	52.8V

Table 12. Ringer load (VPOS = 12 V) with European REN

CREV	Crest factor	1 REN		3 REN	
		Vppk	Vrms	Vppk	Vrms
22nF	1.22	66.4V	54.2V	65.6V	53.2V

3.10.2 With USA REN

If the device has to drive up to 5REN, as requested by USA specifications (1REN = 8 µF + 6930 Ω) it is necessary to modify the value of RD = 2.2 kΩ in order to avoid false off-hook detection (IRTH = 100/RD). The following tables summarize the results @ 20Hz ringing frequency.

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Table 13. Ringer load @ 20 Hz ringing frequency (V_{POS} = 4.5V) with USA REN

CREV	Crest factor	1 REN		3 REN		5 REN	
		Vppk	Vrms	Vppk	Vrms	Vppk	Vrms
22nF	1.22	65.0V	53.2V	62.8V	51.5V	61.2V	50.0V

Table 14. Ringer load @ 20Hz ringing frequency (V_{POS}=12V) with USA REN

CREV	Crest factor	1 REN		3 REN		5 REN	
		Vppk	Vrms	Vppk	Vrms	Vppk	Vrms
22nF	1.22	65.6V	53.7V	63.2V	52.0V	61.2V	50.3V

3.11 Efficiency and power dissipation in flyback configuration

At the fixed CLK frequency (125 kHz), the best DC/DC converter efficiency can be obtained with:

- a good compromise between RDS-ON and the parasitic input/output capacitances value of the NchMOS. For this reason the power Mos STN4NF03L has been chosen.
- a high efficiency, fast recovery diode, like the ST SMBYT01-400, showing a Trr max of 35 ns @ VF = 1 A.
- a transformer suited to DC/DC applications.

The following tables (*Table 15* and *Table 16*) summarize the measurements of the DC/DC converter efficiency, made on an ST board.

The efficiency parameter ηis calculated with the following formula:

$$\eta = \frac{\frac{Idc}{dc} \cdot VBAT}{IVPOStot - IVPOSslic} \cdot VPOS$$

Figure 6. Circuit configuration for DC/DC converter efficiency measurements

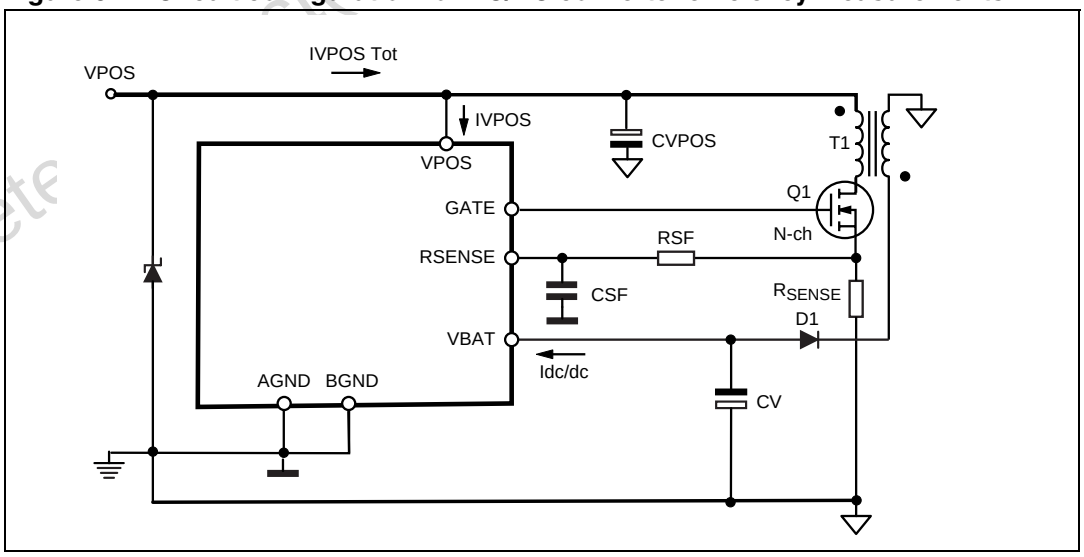

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Table 15. H.I. feeding @ open circuit

VPOS (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	IDC/DC (mA)	VBAT (V)	Pvpos (mW)	Pvbat (mW)	Ratio trafo
4.5	13.80	3.75	0.12	51.8	64.20	5.07	
6	14.10	4.4	0.12	52.0	76.80	5.07	
8.5	14.15	4.13	0.12	52.0	89.59	5.08	1/16
8.5	12.40	4.75	0.12	52.0	58.82	5.08	1/8
12	13.05	4.2	0.12	52.0	96.48	5.08	

Table 16. Active mode @ RLOOP = 500Ω

VPOS (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	IDC/DC (mA)	VBAT (V)	Pvpos (mW)	Pvbat (mW)	Eff% η	Ratio trafo
4.5	205	6.5	29.26	24.5	893.25	716.87	80%	1/16
6	154	7.1	29.28	24.53	881.40	718.24	81%	
8.5	113	7.58	29.3	24.54	896.07	719.02	80%	1/16
8.5	105	7.7	29.34	24.5	827.05	718.83	87%	1/8
12	77.7	8.05	29.38	24.57	835.80	721.87	86%	1/8

Note: Note that for a given value of supply voltage V_{POS}, the current consumption from V_{POS} supply will be influenced by the electrical characteristics of the selected transformer.

3.12 Micro interface

The input levels are interpreted as TTL levels, therefore both 3.3 or 5 V CMOS input signals can be accepted by the STLC3075.

The output DET signal is an open drain (needing an external pull-up resistor to VCC), therefore both 3.3 and 5 V logic levels can be generated, depending on the value of VCC.

3.13 Protection

Different circuit configurations can be used to protect the device from overvoltages.

The best solution to use depends on the specified overvoltage and on whether or not the environment where the STLC3075 has to work is defined by the K20 requirements.

If K20 is requested, a solution that includes a transient voltage suppressor LCP1521, PTC resistors, and two transils has to be used (see *Figure 7*).

Two diodes inside the LCP1521 will clamp to ground any positive lightning, power cross and voltage overstress.

For negative overvoltages, the device will fire because of the gate triggered on the voltage VBAT. A series of two transils (2 x SM6T39A), to best fit the voltage clamp (typically 78 V), will avoid exceeding the total voltage (Vbtot) applied to the device supply pins.

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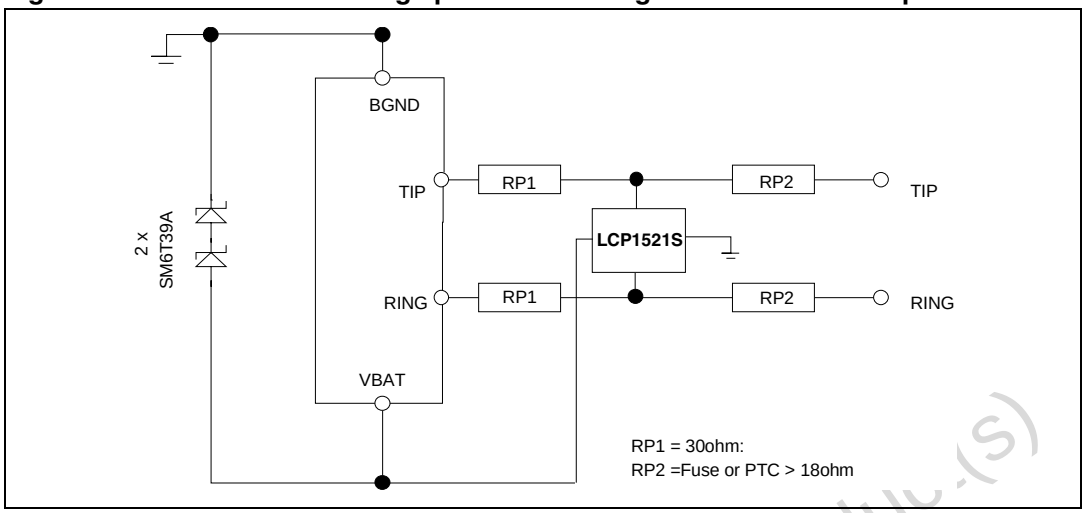
Note: Vbtot = VPOS + VBAT = 90V according to the absolute maximum rating of the STLC3075.

PTC resistors like the Raychem TR250/80T series will prevent damaging during power cross conditions.

Figure 7. Standard overvoltage protection configuration for K20 compliance



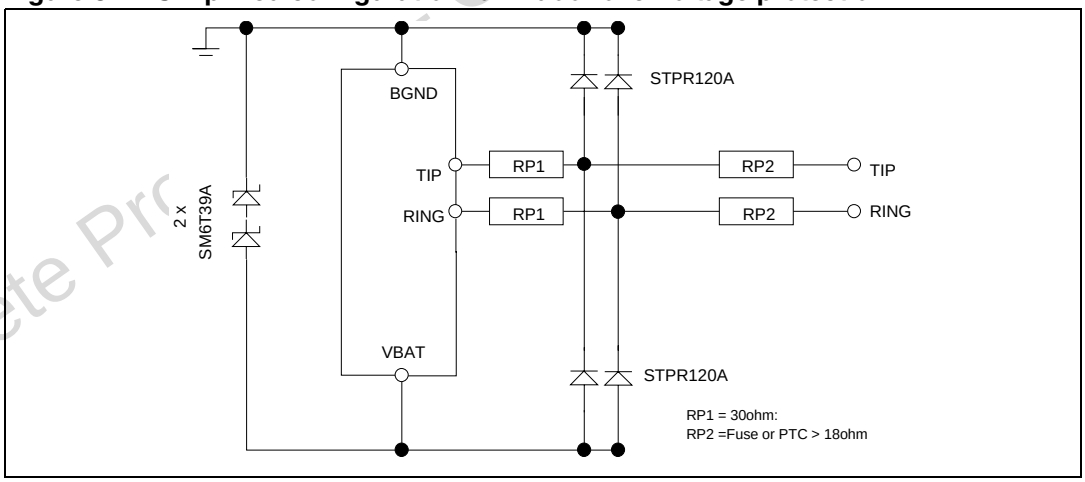
RP1 = 30 Ω and RP2 ≥18 Ω

When K20 requirements are not necessary, a simpler solution consists in the adoption of diodes between VBAT/TIP, RING, TIP, and RING/GND. Suggested diodes are:

- BYT 11-600 or BYW 100-200 for through hole assembly
- STTB 106U or STPR 120A for SMD assembly.

Also in this case, 2 x SM6T39A transils must be used (see *Figure 8*).

Figure 8. Simplified configuration for indoor overvoltage protection



RP1 = 30 Ω and RP2 ≥18 Ω

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3.14 Ring trip

In this SLIC, the ring trip detection is performed by sensing the average current (an image of the line current) injected in the RD resistor, rectified by a dedicated circuit.

It is then filtered by a CAC capacitor and compared to the internally programmed ring trip threshold (IRTH) by the RD resistor itself. Do not confuse this with the RTH resistor which sets the off-hook threshold for active and H.Z. modes.

If the average of the trapezoidal AC current changes in the transition from higher ring impedance (On-hook condition) to low impedance (Off-hook condition), the voltage on the RD resistor increases.

As soon as this voltage goes over the programmed threshold (IRTH), the ring trip will be detected.

In ring mode there is no DC current into the RD resistor, but only the rectified average current. It is clear that the previously described ring trip method is optimized to operate in short loop (<500 Ω) applications and not in the presence of a very long line.

The ring-trip detection threshold is programmed by the formula: IRTH = 100/RD.

With 20 Hz of ring frequency, CAC=22 µF, and RD=4 kΩ, the pin DET goes low about 100 ms after the off-hook transition.

When the SLIC is in ring mode, the maximum average current depends of the REN load. During normal functioning, this current must be lower than the IRTH threshold.

Typical applications can guarantee up to 3REN of load. By increasing the REN number up to 5REN, the AC load will increase. The average current I can then become higher than IRTH and a ring trip will be detected. It is possible to readjust this situation by reducing the value of RD. Alternatively, increasing the IRTH threshold will also increase the ring trip time.

In summary, the ring trip is a function of:

- the load (REN number)
- the value of the ring trip rectified average threshold current "IRTH"
- the value of the maximum peak current sunk from VPOS "Ipk" - higher the REN number lower the value of RSENSE

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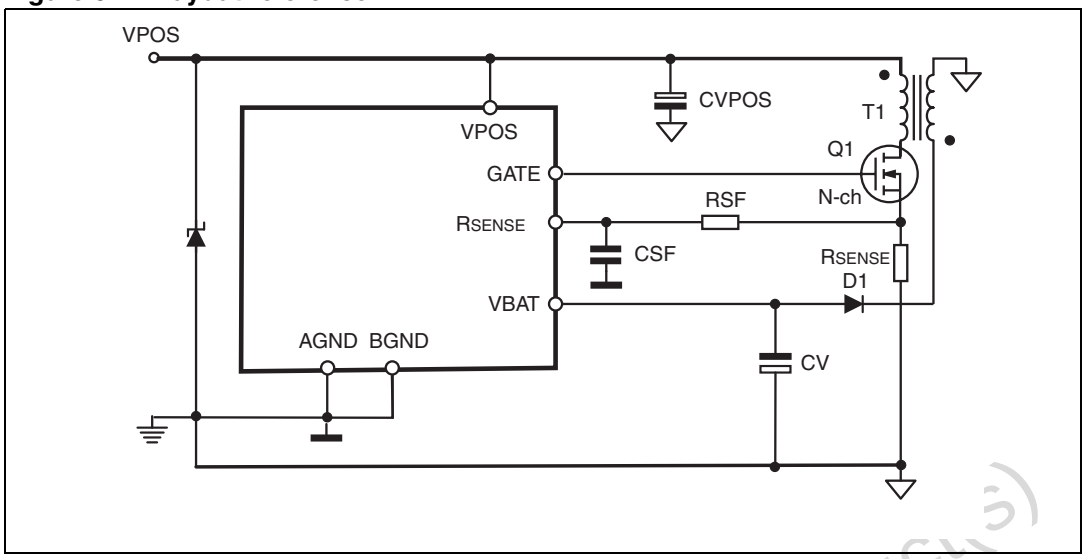
3.15 PCB precautions

Figure 9. Layout reference



Good PCB layout is a basic requirement to avoid noise problems that can have a negative impact on the device operating conditions.

In practice, noise can come from grounding, power supply, parasitic coupling between PCB tracks, and from high impedance points.

The PCB layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (for example: RD, IREF, RTH, RLIM, VF).

As a first recommendation, the components CV, T1, D1,N-MOS, CVPOS, and RSENSE should be kept as close as possible to each other and isolated from the other components.

Noise could be produced by ripple on the CVBAT capacitor and in particular across its equivalent series resistor value (ESR). The lower this value, the lower the ripple that can be present on VBAT.

Particular care has to be taken on the tracks used for connection between VPOS and the DC/DC converter, which must be low impedance tracks due to the high current flowing in them.

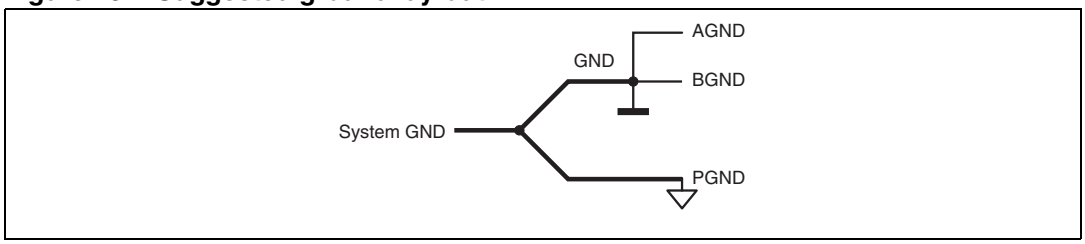
Noise can also be prevented by connecting RREF (26K1) as close as possible to the IREF pin.

Obsolete Product(s) - Obsolete Product(s)

3.16 Ground configuration

Another important point is the ground connection: a star configuration is suggested (see *Figure 10*).

Figure 10. Suggested ground lay-out



It is important to create a specific P-GND area on the layout, with connections to:

- the GND of the CV electrolytic capacitor,
- the GND of the CVPOS electrolytic capacitor,
- the GND of the transformer T1.

This P-GND area has to be connected to the center of the star via a dedicated track.

In this way, any disruptions from the peak current produced by the switching transistor will be cooled by the center of the GND star (system GND), without any disturbance on the other GND (AGND/BGND).

All the other components have to be connected on the GND area.

3.17 Capacitor

Ceramic capacitors CVB and C14 may be used to filter the high frequency ripple and noise that electrolytic capacitors CV and CVPOS respectively are unable to reject.

It is also advisable to connect a 100 nF capacitor from VPOS and GND in order to cancel any high frequency noise on the VPOS pin. This capacitor may not be required, depending on the high frequency sensitivity of the apparatus that the STLC3075 device is included in.

CRD avoids noise coupling on the RD pin, which is a high impedance input.

3.18 On-hook transmission

Voice transmission performances are guaranteed in the complete range of loop currents down to 0mA, when setting the SLIC in active mode, and receiving data on the RX pin during ringing pause.

The maximum output voltage is correlated to the 2 wire overload voltage parameter (see the datasheet).

Obsolete Product(s) - Obsolete Product(s)

3.19 Phone detection

The pin DET can also be used to detect the load status of the line.

When the loop is in on-hook condition with a typical telephone connected, setting the SLIC in active reverse polarity and then changing its status to H.I. feeding, pin DET will go to low level for a time of about 1.5 ms. If the line is open, this time is reduced to about 2 µs.

3.20 ESD immunity

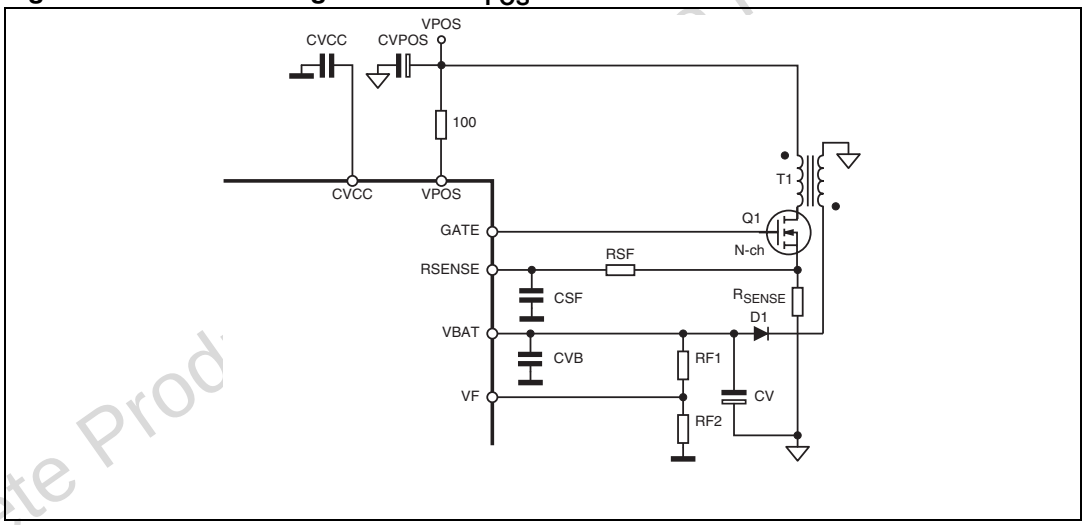
The ESD protection in this device withstands a discharge of 2kV with the Human Body Model. If the STLC3075 must operate in sensitive apparatus where equipment tests against ESD immunity are required (4kV, 8kV), some precautions have be taken.

During these tests, where the device is usually powered, ESD transients can put the internal ESD protection diodes (connected on VPOS and RSENSE pins) into the ON condition.

When the transient disappears and the VPOS supplied is higher than 9 V, the internal ESD diodes are not able to recover back to the OFF condition.

Using a VPOS supply of less than 9 V, the recovery of the ESD diodes is guaranteed and the equipment will be able to pass the ESD immunity tests. When it is not possible to use a reduced VPOS voltage, a solution can be found by putting a 100 Ω resistor in series at pin VPOS, without any impact on the threshold of the input limitation circuit.

Figure 11. Circuit configuration for V_{POS}>9V



Obsolete Product(s)

3.21 Setting resistor

The following current is flowing into the resistor of the STLC3075 application:

- IRLIM, IRTH, IRREF = 1.3 V/R
- IRD = Iline/100
- IRSENSE = 100 mV/RSENSE
- IRF1, IRF2 can be considered around 300 µA
- No DC current flows into RS, ZAC, ZA, ZB, RLV, RTTX.

3.22 Longitudinal balance

To avoid degradation on this parameter, it is very important to use Rp resistors with 1% tolerance, and (if used) PTC resistors with 1% matching.

Low longitudinal balance rejection, caused by the mismatching of the resistors or PTC, can generate noise problems. For example in a GSM based WLL, noise can be generated from the 25 Hz produced by the 4 ms burst of the antenna transmission.

3.23 TTX filter

A dedicated metering pulse low pass filter (12 kHz to 16 kHz), with 3rd order filtering can be obtained by choosing the following values for the external components:

RLV=16K2//16K2 =8.1K, CFL=1.5 nF, R1=1.3 MΩ, R2=180K, C1=47 pF, C2=6.8 pF.

If the TTX is not requested, the components RLV, CS, CFL, RTTX, CTTX can be removed. In addition, the pins CKTTX, CTTX1, CTTX2, FTTX have to be connected to GND, and the pin RTTX open.

3.24 Gain settings

In order to adapt the SLIC versus the 3.3 V low supply voltage CODEC, the device provides the possibility to change the TX and RX gains by the gain set control pin.

Table 17. TX and RX gains by the gain set control pin

Gain set	RX gain	TX gain	Impedance synthesized scale factor
0	0dB	- 6dB	X 50
1	+ 6 dB	- 12dB	X 25

3.25 Complex impedance

Most countries (administration) adopt complex impedance for both the “Exchange Impedance” (Zexch) and the “Balance impedance”, instead of a 600 Ω purely resistive impedance. As a consequence, the AC input impedance that the SLIC plus protection resistor shows at its line terminals (Zs), has to be calculated in order to correctly match the Zexch, to obtain good performance on the return loss parameter.

When Zexch is a complex impedance, the synthesized impedance Zs will be calculated as:

$$Zs = \frac{ZAC}{50} + 2Rp$$

where 50 is a fixed scale factor. (For ZAC definition see datasheet.)

For gain set = 1 the scale factor is 25.

Considering, for example, the ETSI 2 complex impedance Zexch = 270 + (750//150nF).

Obsolete Product(s) - Obsolete Product(s)

An AC input impedance has to be synthesized on pins TIP/RING of the SLIC (ZAC), to do so, considering the line terminal, the proper Zs have to be calculated as:

- ZAC =(Zs-2Rp)*50 because 2Rp = 100 Ω
- ZAC = (270-100)*50 + [(750*50)//(150 nF/50)] = ZAC = 8.5K + (37.5K//3 nF)

In this way the SLIC will synthesize Zs impedance matching correctly the Zexch.

Also for the 2 to 4 wire conversion, the administration defines an AC terminal balance impedance Zb properly used to obtain the THL performance.

Good trans-hybrid loss performance, and therefore proper echo cancellation, can be obtained by correctly matching the two external impedances, ZA and ZB, which can also be complex impedances.

ZA = 50 x Zexch

ZB = 50 x Zb

For gain set = 1, the scale factor is 25.

In case of Zb = Zexch, the impedances ZA and ZB can be replaced by two resistors calculating their value as:

ZA = ZB = 50 x |Zexch|. For gain set = 1 the scale factor is 25.

Where |Zexch| is the modules @ 1 kHz.

For ETSI 2 the value |Zexch| = 842 Ω

ZA = ZB = 50 x 842 Ω = 42.1 kΩ

A typical value of 120 pF (with gain set = 0) for the capacitors CComp and CH guarantee both the loop stability and good THL performance.

For gain set = 1 the capacitor value is doubled.

Obsolete Product(s) - Obsolete Product(s)

4 Support

Please contact your local ST sales office for details of the STLC3075 firmware.

5 Revision history

Table 18. Document revision history

Date	Revision	Changes
09-Jun-2006	1	Initial release.
09-Jun-2006	2	Updated *Section 3.7*. Added *Appendix A* and *Appendix B*.
19-Feb-2007	3	Updated *Figure 3*. Added references to Coilcraft in *Table 4* and added *Table 5* and *Table 6*.

Obsolete Product(s) - Obsolete Product(s)

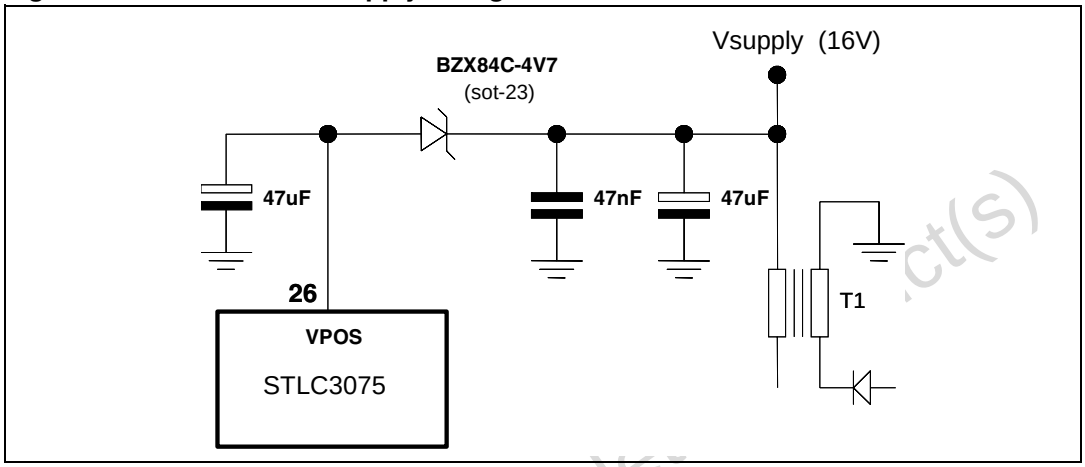
Appendix A STLC3075 in application with VPOS > 12 V

In a typical application the STLC3075 can operate correctly up to a 12 V VPOS voltage.

Using the Fly Back configuration, and by modifying the typical circuit configuration by just adding a zener diode or a voltage regulator, it is possible to provide the right voltage to VPOS (pin 26) in order to get a voltage lower than 12V.

Using this circuit configuration it is necessary to use a MOSFET type STN3NF06L with a VDS of 60V.

Figure 12. STLC3075 for supply voltage >12 V



Obsolete Product(s) - Obsolete Product(s)

Appendix B STLC3075 for USB suspended current specification[a]

In Power Down or H.I. mode, the current consumption from VPOS by the STLC3075 is about 12 mA. By turning off the DC/DC converter, pin CLK to GND, this value is reduced to about 4 mA.

In a USB bus-powered device, the total current taken from the USB bus has to be no more than 500 µA (see USB 2.0 para 7.2.3). To meet this specification, the only possibility is to turn-off the SLIC.

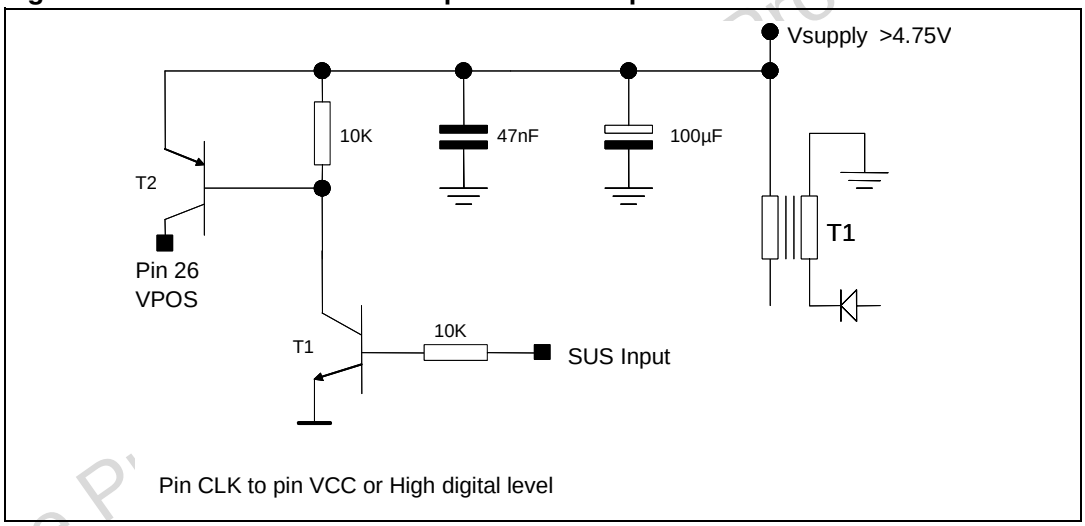
One possible way to do that is shown in the schematic below.

Adding a few components, and using the STLC3075 in Fly-back configuration, it is possible to meet this specification up to 4.75 V supply voltage, considering 250 mV as a max Vdrop of T2.

The STLC3075 can be set in self oscillation mode, hardware connecting pin CLK to pin CVCC.

A digital command, logic level High, connected to the SUS input will enable the two transistors T1 and T2 to provide the correct power supply to the pin 26 of the SLIC.

Figure 13. STLC3075 for USB suspend current specification



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a. Current consumption < 1mA

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